THIN FILM OPTICAL WAVEGUIDES IN III-V SEMICONDUCTORS

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13. ABSTRACT

The development of techniques for the growth of vapor phase epitaxial GaAs/GaAsP waveguide structures, and GaAs/GaAlAs structures in which the GaAs layer is grown by vapor phase epitaxy on a GaAlAs liquid phase epitaxial substrate are described. Large area GaAs/GaAsP structures with good surface quality have been achieved, but wafer bow problems due to lattice mismatch have prevented the accurate measurement of attenuation rates.

Two dimensional waveguides have been fabricated which have attenuation rates comparable to one dimensional waveguides. This result suggests that it should be possible to fabricate a two dimensional electro-optic modulator with a relatively low drive power.

KEY WORDS: Gallium arsenide, Gallium arsenide phosphide, Gallium aluminum arsenide, Vapor phase epitaxy, Liquid phase epitaxy, Integrated optics, Thin film wave-guides, Electro-optical modulation, Optical attenuation

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FOREWORD

This semi-annual technical report covers the work performed under contract F19628-72-C-0324 between the period July 1, 1973 to December 31, 1973.

The objective of this program is to grow a variety of epitaxial GaAs, GaAsP and GaAlAs waveguide structures and to evaluate their performance with regard to the propagation of 10.6μm radiation. The effect of such parameters as layer thickness, alloy composition profile, and carrier concentration will be investigated. Vapor phase epitaxial techniques are being employed to grow the GaAsP structures and liquid phase epitaxial techniques have been used to grow the GaAlAs structures.

Technical direction is being provided by Dr. Andrew Yang of the Air Force Cambridge Research Laboratory. The growth of the epitaxial structures is being carried out in the Monsanto Commercial Products Company, Electronic Products Division, Laboratories, St. Louis, Missouri, and the waveguide evaluation has been subcontracted to and is being performed in the laboratories of the Washington University School of Engineering and Applied Sciecne, St. Louis, Missouri.

The research carried out on this program is under the direction of M. George Craford. Others directly involved in this work and in the preparation of this report are D. Finn, W. O. Groves, and A. H. Herzog, of Monsanto Company, and W. S. C. Chang, M. Muller, and M. S. Chang, of Washington University.

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1.0 SUMMARY OF RESULTS

1.1 Vapor Phase Epitaxy (VPE)

Growth conditions have been developed which produce GaAs/GaAsP epitaxial structures with good surface quality. However, the surface of the wafers were bowed due to lattice mismatch between the GaAs and GaAsP layers. This bowing was not unexpected and it is anticipated that it can be eliminated by properly adjusting the alloy composition profile during the growth of the epitaxial structure.

Growth conditions were developed, after considerable difficulty, which resulted in GaAs (VPE)/GaAlAs (LPE) structures with fair surface. However, the growth of this type of structure is more complicated, and is viewed to be much less promising, than the growth of GaAs/GaAsP epitaxial structures.

1.2 Liquid Phase Epitaxy (LPE)

It has been decided to indefinitely suspend the LPE portion of this program and to concentrate the full effort on the VPE work. This decision is based on the fact that the attenuation rates of 1-2 db/cm which have been obtained in this program on GaAs/GaAsP structures are at least as low as any obtained on GaAs/GaAlAs structures. Furthermore, the materials technology, for the growth of the large area films which will be required for the reproducable production of usable devices, is much more advanced for VPE growth than for LPE growth.

1.3 Evaluation

No detailed attenuation measurements were obtained on GaAs/GaAsP structures due to the surface bow effect. However, preliminary results indicate that when the bow is eliminated high performance structures should be obtained.

Experimental fabrication of two-dimensional waveguides were successful. The attenuation rate for a two-dimensional waveguide as low as for a one dimensional waveguide is achievable.

Theoretical calculation of the r.f. power dissipation of an electro-optic modulator has been initiated.

2.0 VAPOR PHASE EPITAXY

2.1 Introduction

The objectives of the Vapor Phase Epitaxy (VPE) portion of this program are to grow various n/n^+ GaAs, $GaAs/GaAs_xP_{1-x}$, and $GaAs_xP_{1-x}/GaAs/GaAs_xP_{1-x}$ structures to determine the effect of various parameters including film thickness, carrier concentration and alloy composition on waveguide properties at 10.6 μm. In addition to structures of the first two types grown during the third portion of this program, some work has also been done on $GaAs/Ga_xAl_{1-x}As$ structures. However, the work carried out to date on this program has yielded attenuation rates of 1-2 db/cm which are at least as low as the best rates yet achieved in the $Ga_xAl_{1-x}As$ system where an attenuation rate of 2 db/cm for the TE_0 mode has been recently obtained(1). Thus, since the materials technology for the $GaAs_{1-x}P_x$ system is far more advanced than that for the $Ga_xAl_{1-x}As$ system, we have decided to concentrate our efforts on the $GaAs_{1-x}P_x$ system and to suspend indefinately our work on the $Ga_xAl_{1-x}As$ system.

2.2 Results Obtained in Production Scale VPE Reactors

2.2.1 n/n^+ GaAs

Success in achieving low carrier concentrations in the $10^{14}/cm^3$ range in n/n^+ GaAs by proper adjustment of growth parameters was reported in the previous Semi-Annual Technical Report. Surface quality, however, remained a problem. During this period, by careful attention to substrate preparation and adjustment of starting conditions, several large wafers of excellent surface quality have been produced. The results, however, have not been completely reproducible.

Initially, small substrate wafers were used in runs made to solve the epitaxial surface problems under conditions also designed to yield low free carrier concentrations. After thirteen runs in which measurable free carrier concentrations and mobilities averaged 3×10^{15} cm^{-3} and 4400 cm^2/volt-sec, respectively, a crack was discovered in an inlet tube to the reactor. Subsequently the data shown in Table I was obtained, comparable to that shown previously in Table V of the last Semi-Annual Technical Report. In general good surfaces were obtained on the small GaAs substrate pieces whereas much poorer surface quality was obtained on large full size wafers. In part this could be attributed to poorer structural quality of some of the large GaAs ingots and in part related to reactor geometry. Various modifications of cleaning procedures and the use of silica back coated wafers were tried with inconclusive results, but ultimately some very good layers of large surface area were obtained.

Similar data for thin epi GaAs layers, shown in Table II, show much less consistency than the thicker layers of Table I. This problem will be discussed more fully below.

2.2.2 $GaAs/GaAs_xP_{1-x}/GaAs$

As reported in the last semi-annual technical report, it has been possible, by using appropriate wafer cleaning and start up conditions, to grow GaAs layers on $GaAs_xP_{1-x}/GaAs$ wafers with surface quality equivalent to the original $GaAs_xP_{1-x}$ surface. Standard Hall constant and resistivity measurements made on GaAs layers grown on companion semi-insulating GaAs substrates have proved unreliable but capacitance-voltage (C-V) measurements indicate low free carrier concentrations in this material. Data are listed in Table III. The carrier concentrations obtained from zero-bias capacitance (C_0) are upper limits, since the zero-bias depletion depth measured is essentially the thickness of the layer.

Prior to the growth of $GaAs/GaAs_xP_{1-x}/GaAs$ structures, several runs were made to determine the characteristics of the $GaAs_xP_{1-x}$ layer and to attempt to minimize the carrier concentration. The data shown in Table IV indicate that for good surface quality, the deposition temperature must be increased to about 820°C, resulting in free carrier concentrations in the $10^{16}/cm^{-3}$ range.

$GaAs/GaAs_xP_{1-x}/GaAs$ structures of good surface quality have been grown in either single, continuous runs, or in two separate runs. In the former case, growth is actually discontinued for a period while furnace temperatures are reduced from those required to grow good quality $GaAs_xP_{1-x}$ to those necessary for low carriers in the GaAs layer. In the latter case an additional semi-insulating GaAs substrate may be included in the second run to provide a sample of the epi GaAs growth alone for Hall and resistivity measurement. Data are summarized in Table V and VI. Mobility data for the composite layers are not included because such mobilities are dominated by the high mobility region of the initial graded layer and do not reflect that of the ~ 38% GaP alloy layer[2]. Carrier concentrations also are affected and may be considered to be about a factor of two higher than listed, as is shown by the CV data obtained for Run No. 484, listed in Table IV.

As shown in Tables V and VI, the net electrical carrier concentration of the GaAs layer, as determined by Hall measurement for these runs, has not been brought below $10^{15}/cm^3$. This is due to other system problems, however, and not to the presence of the $GaAs_{1-x}P_x$ growth, as is demonstrated by subsequent failure to obtain low carrier concentration in GaAs/GaAs alone. Also good surface quality and low

carrier concentrations, in the $10^{-14}/cm^3$ range, had been achieved earlier for GaAs layers grown on production samples of $GaAs_xP_{1-x}$ red LED material.

It is now suspected that reactor conditions, adopted for the start up of GaAs layer growth, cause the formation of a heavily doped layer at the interface. This would result in a spuriously high carrier concentration and low mobility for a Hall sample on a semi-insulating substrate. Such an interfacial layer would not be distinguished from the substrate by a normal C-V measurement but in an extreme case might be observed. The C-V results obtained by step-etching one thin $GaAs/GaAs_xP_{1-x}/GaAs$ structure, Run No. 481, Table V, might be accounted for in this way, lending support to the argument.

Thus, the electrical evaluation of thin epi layers of low carrier concentration is a continuing problem. In addition to the above difficulty, sporadic occurrence of p-type Hall readings (Tables II and III) which render suspect all measurements of carrier concentration below about $10^{15}/cm^3$, have tentatively been attributed to Cu contamination of the semi-insulating Cr doped GaAs substrate. Spectroscopic analysis of samples from two different lots of Cr doped GaAs showed Cu concentration of 1.7×10^{16}a$/cm^3$ and 4.9×10^{14}a$/cm^3$ respectively. Rapid diffusion of Cu from the substrate into the epi layer of the Hall sample at growth temperatures of ~750°C could easily convert this layer to p-type while not affecting the n-type growth on other substrates in the run. In addition to the possibility of this type of contamination, is the difficulty of making low resistance ohmic contacts to low carrier concentration material. Reliable contacts to material of much less than 10^{14} carrier$/cm^3$ have not been domonstrated.

Capacitance-voltage (C-V) measurements alsc lose some of thier utility for thin layers of low carrier material because of the dependence of the zero-bias depletion depth in a Schottky junction on carrier concentration. At 5×10^{13} carrier$/cm^3$ in GaAs this is already about 5 μm, the thickness of the active layer. In practice, excessive leakage has prevented accurate C-V measurements under forward bias to obtain data at depths much less than the zero-bias depth. Thus only an estimate of an upper limit to the carrier concentration can be obtained from the zero-bias capacitance.

While, as indicated above, excellent surface quality has been achieved for both n/n^+ GaAs and $GaAs/GaAs_xP_{1-x}/GaAs$ structures, in the latter case, the very large area wafers have been bowed so as to prevent efficient prism coupling in waveguide tests.

The bowing of the wafers is thought to be due to residual strain not releaved by the generation of mismatch dislocations. The strain arises from mismatch of the lattice spacing of successive layers of alloy of changing composition[2]. Since a finite stress is required to generate dislocations, the actual lattice spacing for a given layer in the graded region tends to lay below the normal unstrained spacing for that composition resulting in bow, concave upwards in the case of the smaller GaP richer alloy growing on GaAs. If the grading process is discontinued just when the desired alloy composition is reached, insufficient mismatch dislocations will have been generated to accomplish the overall change in lattice spacing between GaAs and the final $GaAs_xP_{1-x}$ composition. The resulting strain produces an appreciable bow in the wafer. The strain and bow can be compensated by generating additional dislocations. This can be done simply by grading beyond and then dropping back to the desired composition. In this case, ideally, the lattice spacing of the upper most layer of the graded region with higher phosphorous content will just correspond to that of the desired composition. Residual atomic strain will be confined to the graded region leaving the bulk of the substrate and epitaxial layer unstrained and flat. In practise, it is easy to produce bowing in either direction or to eliminate it for ordinary masking purposes in planar processing. The exact solution may be more difficult for complex waveguide structures with stringent flatness requirements. Although the rate of change of reactant concentrations can be programmed and controlled accurately, the actual growth rate and thus the concentration gradient varies considerably from run to run due to uncontrolled factors.

The degree of control of bowing that can be achieved must be determined. Initially attempts will be made to establish a slightly convex rather than a concave bow. This should simplify prism coupling.

2.2.3 $GaAs/Ga_xAl_{1-x}As$

Exploratory runs for growing films of GaAs on GaAlAs substrates were attempted using <100>oriented substrates obtained from Monsanto Electronic Special Products. While layers grown simultaneously on GaAs for Hall samples were of good quality, equivalent to those listed in Tables I and II, very poor epi layers were grown on the GaAlAs. This was to be expected from the poor quality of the substrate surfaces and the tendency of pyramids to grow on near <100> surfaces. Subsequently LPE layers grown 2° off < 100 > were obtained in the LPE portion of this program. Since LPE growth on off-orientation substrates produces a step-like surface, it was necessary to lap and polish the wafers before using them in an attempt to grow planar VPE films.

The best VPE GaAs surfaces using standard growth conditions were rather dull and contained pronounced growth steps as evident in Figures 1 and 2. This result is believed due to initial nucleation and growth of discrete islands whose edges continue to grow as steps even after overlapping. It resembles growth on a very rough or pitted surface even though the interface is flat. A more extreme case is shown in Figure 3a and b, in which prior to growth the substrates were vapor etched for two minutes in the presence of AsH_3. This treatment evidently effectively masked the surface and delayed nucleation and growth of GaAs except along surface scratches. The size of the growth islands much be related to the time of nucleation. These effects are thought to be related to the stability of aluminum oxide and the greater tendency of GaAlAs to form a stable oxide surface.

Some improvement in nucleation was achieved by increasing the deposition temperature, but the best results were obtained by increasing both temperature and total gas flows and switching directly into the growth cycle after bringing the substrates to temperature under hydrogen flow. After a total of twenty-three runs, a fairly good GaAs layer was obtained on a large (3/4" x 1" plus) GaAlAs substrate in the twenty-fourth run. Table VII summarises the results.

Due to the inherent difficulty in combining VPE processing with LPE, differences in preferred growth orientation, additional handling required and critical nature of the substrate surfaces, this approach is being abandoned in favor of concentration on the GaAs/$GaAs_xP_{1-x}$/GaAs structures. The latter is suited to and requires an all VPE process, whereas GaAs/GaAlAs structures can and are being grown in all LPE systems elsewhere. Furthermore, as mentioned earlier, the attenuation results obtained in this program using $GaAs_xP_{1-x}$ sturctures are at least equivalent to any obtained using GaAlAs structures so there is no strong incentive to try to cope with the difficulties presented by the large area LPE growth of GaAlAs.

2.3 Waveguide Structures Submitted for Evaluation

The GaAs n/n^+, GaAs/GaAsP and GaAs/GaAlAs waveguide structures which have been submitted for evaluation to Washington University during the past six months are summarized in Table VIII, Table IX, and Table X, respectively. Evaluation of the samples is described more completely in Section 4.0.

2.4 Conclusions

1. Growth conditions have been developed which can produce GaAs films of good surface quality on large area GaAs substrates with carriers in the low $10^{14}/cm^3$ range or lower.

2. Growth conditions have been developed which produce GaAs films of good surface quality on large area GaAsP substrates.

3. A high carrier concentration, low mobility layer may be produced at the GaAs/GaAsP interface which obscures electrical evaluation. Carrier concentrations in the bulk of the GaAs layer may be in the $10^{13}/cm^3$ range.

4. Carrier concentrations in the GaAsP layer are in the 10^{16} cm^{-3} range.

5. Due to possible interference from interfacial layers of copper contamination, Hall measurements of low carrier concentration in thin layers have not been reliable.

6. Growth of GaAs/$GaAs_xP_{1-x}$/GaAs structures tends to produce excessive bowing of large area wafers, preventing efficient prism coupling in waveguide evaluation.

7. Growth conditions have been developed which can produce GaAs films of fair surface quality on GaAlAs substrates with some sacrifice in carrier concentrations.

8. VPE growth of GaAs on LPE GaAlAs substrates requires mechanical lapping and polishing of the off-orientation LPE epi surface.

TABLE I

Undoped Epitaxial GaAs Grown at Modified Ga/As/HCl Growth Conditions

Run No.	Deposition Temp, C	Net Carriers n, cm^{-3}	Mobility, μ cm^2/volt-sec	Epi Film Thick μm	Surface Appearance
394	748	2.9×10^{15}	4670	29.6	Few pyramids(1)
395	749	6.4×10^{14}	6600	24.7	
396	753	3.9×10^{14}	7690	23.5	Very good(1)
397	747	1.2×10^{15}	6670	23.4	Very good(1)
398	750	3.7×10^{15}	4950	19.8	
399	747	2.1×10^{15}	5800	27.1	
400	754	4.9×10^{14}	7510	22.0	
401	751	2.1×10^{14}	7680	21.8	Very pitted(2)
402	749	4.0×10^{14}	6880	23.0	
403	754	2.7×10^{14}	7600	21.5	Scattered pits(2)
404	751	4.1×10^{14}	7470	22.0	
405	750	2.7×10^{14}	7250	21.1	
406	749	3.3×10^{14}	7060	23.2	
421	754-744	2.9×10^{14}	7717	21.1	
422	749	3.5×10^{14}	7490	25.4	Very good(2)
423	744	6.9×10^{14}	6079	23.7	
424	744	No readings		21.5	
425	744	4.7×10^{14}	6690	23.4	

(1) Small area substrate wafers

(2) Large area substrate wafers

TABLE II

Undoped Epitaxial GaAs Grown at Modified Ga/As/HCl Growth Conditions

Run No.	Deposition Temp C	Net Carriers n, cm^{-3}	Mobility, μ cm^2/volt-sec	Epi Film Thick, μm	Surface Appearance
407	749	9.8×10^{14}(p)	331	4.9	Excellent
408	750	p and n Hall voltages		~ 5	
409	747	1.3×10^{15}	6452	5.6	
410	253	3.6×10^{14}	6341	5.8	
411	750	1.6×10^{14}(p+n)	739	5.5	
412	752	$2.-1 \times 10^{14}$	7349	5.8	
413	757	4.6×10^{14}(p)	205	6.2	
414	749	8.1×10^{14}	6068	4.9	
415	753	4.3×10^{14}	5837	5.5	
416	752	1.1×10^{13}	7077	5.7	
417	740	1.3×10^{15}	4531	6.0	
418	743	1.1×10^{15}	5112	5.5	
419	740	7.8×10^{14}	5765	5.7	
420	738	1.46×10^{15}	6135	5.9	
426	745	4.7×10^{14}	6650	6.2	
427	745	3.1×10^{14}(C-V) 1.4×10^{14}($C_{0.5}$)	--	5.5	
428	758	5.6×10^{14}(C-V) 4.8×10^{14}($C_{0.83}$)	--	4.9	

TABLE III

Undoped Epitaxial GaAs Grown on LED $GaAs_xP_{1-x}$/GaAs Material

Run No.	Deposition Temp. °C	Net Carriers n, cm^{-3}	Mobility, μ cm^2/volt-sec	Epi Film Thick, μm	Surface Appearance
453	786	7.6×10^{15}	5590	18	Hazy
456	788-741	2×10^{15}	5340	5.9	
457	757	No readings		6.2	
458	757	3.4×10^{14}	3680	5.8	Good
		4.2×10^{14}(CV)			
459	760	4.2×10^{14}(p)	188	2.5	Hazy
460	748	No stable readings		--	Good
		2.4×10^{14}(CV)		13.9	
		4.4×10^{14}(C_0)			
461	746	8.1×10^{14}	5520	4.7	Good
462	748	8.6×10^{13}	1306	4.9	Good
		6.6×10^{13}(C_0)		4.9	
463	744	5×10^{15}	4040	--	Good
		6.8×10^{13}(C_0)		4.7	
464	748	5.0×10^{14}	5103	6.2	Good, scattered specks
		4.9×10^{13}(C_0)		6.5	
465	747	5.3×10^{13}	2189	7.8	Fairly good, some faults
		4.5×10^{13}(C_0)		6.0	
466	736	7.8×10^{13}	3779	7.8	Rows of faults
		3.4×10^{13}(C_0)		7.1	

TABLE III (Continued)

Run No.	Deposition Temp°C	Net Carriers n, cm^{-3}	Mobility, μ cm^2/volt-sec	Epi Film Thick. μm	Surface Appearance
467	737	1.5×10^{13}	8801	~ 7	Poor, many faults
468	748	No readings		---	Poor, many faults
		$6.4 \times 10^{13}(C_0)$		5.2	
469	749	5×10^{14}(p)	137	5.9	Rows of faults
470	758	7.3×10^{14}(p)	203	5.9	Rows of faults
471	760	No readings		---	Very bad

TABLE IV

Undoped $GaAs_xP_{1-x}$ Growth

Run No.	Deposition Temp. °C	Thickness, μm Grade	Alloy	Net Carriers n, cm^{-3}	Surface Quality
472	793	44.5	59.3	1.07×10^{16}	Bad, pyramids, faults
473	806	24.7	29.6	1.4×10^{16}	Many faults some areas
474	805	14.8	31.1	2.3×10^{16}	Few pyramids, many faults
475	810	99	108	7.4×10^{15}	Fairly good
476	817	39.5	64.2	3.5×10^{16}	Solvent stain traces
477	818	59.3	54.3	4.6×10^{16}	Debris on surface
478	818	24.7	34.6	5.3×10^{16}	Very good, some debris
479	818	50.9	64.2	3.0×10^{16}	Very good
484	819	31.2	40.0	3.5×10^{16}	Good
				7.2×10^{16}	CV (to depth of 0.45 μm)
490	816	39.5	39.5	5.1×10^{16}	Good
492	816	34.6	29.6	4.9×10^{16}	Verry good, 2.39 in^2

TABLE V

Undoped GaAs/$GaAs_xP_{1-x}$/GaAs Grown in Single Run

Run No.	Layer Thickness, μm			Net Carriers(1) n, cm^{-3}	Surface Quality
	Grade	Alloy	GaAs		
480	32.1	51.9	3.9	2.2×10^{16}	Good
			2.9	$2.6 \times 10^{14}(C_0)$	
481	47.8	48.8	4.9	9.4×10^{15}(2)	Much debris
			3.8	$9.4 \times 10^{13}(C_0)$	
482	29.1	32.6	5	1.7×10^{16}	Good, few pieces debris
489	34.1	34.6	10	7.6×10^{16}	Rough, 2.20 in^2
493	33.2	29.3	7.8	4.8×10^{16}	Good, bowed
6-1	39.5	29.7	9.6	4.6×10^{16}	Excellent, bowed, 3.91 in^2
6-5	24.6	29.5	7.8	3.7×10^{16}	Very good, bowed
6-8	45.2	28.5	10.7	3.3×10^{16}	

(1) Hall measurement includes complete composit layer including graded region, alloy and GaAs layer; C_0 measurement gives upper limit to carrier concentration of GaAs layer.

(2) Hall measurement of composit layer; CV measurement of wafer at surface and after removing 3.5 μm indicates peak carrier concentration of $2.5 \times 10^{17} cm^{-3}$ in a layer approximately 0.1 μm wide at or near the interface.

TABLE VI

Undoped GaAs/$GaAs_xP_{1-x}$/GaAs Grown in Two Separate Runs

Run No.	Layer Thickness, μm Grade	Alloy	GaAs	Net Carriers[1] n, cm^{-3}	Mobility, μ[2] cm^2/volt-sec	Surface Quality
6-2	22.4	35.1	6.8	7.8×10^{16}	----	Speckled
			6.8	1.3×10^{15}	6755	
6-3,4	39.3	24.6	5.9	4.9×10^{16}	----	
			5.9	1.2×10^{15}	4967	
6-6,7	26.4	25.6	2.0	4.5×10^{16}	----	Few streaks and pits
			2.0	1.8×10^{15}	6343	

(1) 1st value is from Hall measurement of composite layer grown in both runs. 2nd value is for GaAs layer only, grown on semi-insulating substrate added for 2nd run.

TABLE VII

Undoped GaAs Grown on GaAlAs

Run No.	Deposition Temp, C	Net Carriers n, cm^{-3}	Mobility, μ cm^2/volt-sec	Film Thick, μm	Surface Quality
433	754	1.07×10^{14} 2.3×10^{14}(C-V 7.3×10^{13}($C_{0.5}$)	7500	7.8 13	Poor
434	757	7.5×10^{13} 6.0×10^{14}(C-V) 3.1×10^{13}($C_{0.6}$)	7427	6.8 4	Poor
435	756	p + n readings 2.9×10^{4}(C-V) 5.5×10^{13}(C_0)		12.7 9.5	Poor
436	755	4.9×10^{14}	5027	5.8	Poor
437	756	1.0×10^{15}	4601	5.8	Poor
438	756	6.5×10^{12}(V. unstable	2030	7.8	See Figure 1
439	770				See Figure 2
440	738	3.8×10^{14}	7126	14.6	See Figures 3a and b
443	747	7.8×10^{11} (V. unstable) 4.2×10^{14}(C-V) 5.4×10^{14}(C_0)	2814	5.8 5.4	Poor
447	776	4.4×10^{15}	5527	12.1	Better, but contains pits
448	784	9.1×10^{14}	7179	13.8	Stacking faults
449	793	1.3×10^{15}	6162	13.7	Stacking faults
450	784	6×10^{14}	6825	15.6	Very good - few pits
451	798	1.1×10^{14}	5893	13.8	Good, few faults and pits
452	790	1.9×10^{15}	5980	7.8	Fairly good, Large Area

Runs 448 through 452 at twice normal flow rate
Hall and C-V measurements on GaAs substrates

TABLE VIII

GaAs n/n+ Structures Submitted for Evaluation

Sample Number	Film Thickness μm	Film Carrier Conc. cm^{-3}	Substrate Carrier Conc. cm^{-3}	Remarks
VR5-415	5.5	4.3×10^{14}		For two-dimensional waveguide evaluation
VR5-416	5.7	1.1×10^{13}		"
VR5-417	6.0	1.3×10^{15}		"
VR5-421	21.1	2.9×10^{14}		"
VR5-422	25.4	3.5×10^{14}		"
VR5-423	23.7	6.9×10^{14}		Submitted to AFCRL for ion implantation.
VR5-424	21.5	-----		For two-dimensional waveguide evaluation.

TABLE IX

GaAs/GaAsP Structures Submitted for Evaluation

Sample Number	Film Thickness μm	Film Carrier Conc, cm^{-3}	Substrate Carrier Conc, cm^{-3}	% P	Remarks
VR5-489	10	$\sim 10^{14}$	7.6×10^{16}	~ 38	Rough Surface
VR5-493	7.8	$\sim 10^{14}$	4.8×10^{16}	~ 38	Bowed Surface
VR6-1	9.6	$\sim 10^{14}$	4.6×10^{16}	~ 38	Cracked while sawing
VR6-3	5.9	1.2×10^{15}	4.9×10^{16}	~ 38	Bowed Surface
VR6-5	7.8	$\sim 10^{14}$	3.7×10^{16}	~ 38	< 4 db/cm loss Bowed Surface.

TABLE X

GaAs/GaAlAs Structures Submitted for Evaluation

Sample Number	Film Thickness μm	Film Carrier Conc. cm^{-3}	Substrate Carrier Conc. cm^{-3}	PL* Wavelength Å	Remarks
VR5-436	5.8	4.9×10^{14}	1.5×10^{16}	7100	Small Samples used for surface planarity measurements.
VR5-437	5.8	1.0×10^{15}	5.8×10^{16}	6900-7100	"
VR5-452	7.8	1.9×10^{15}	2.2×10^{16}	6800-7100	Not yet evaluated.

*PL = Photoluminescence at surface of original epi-layer (300K) or after etch polishing to remove surface Ga.

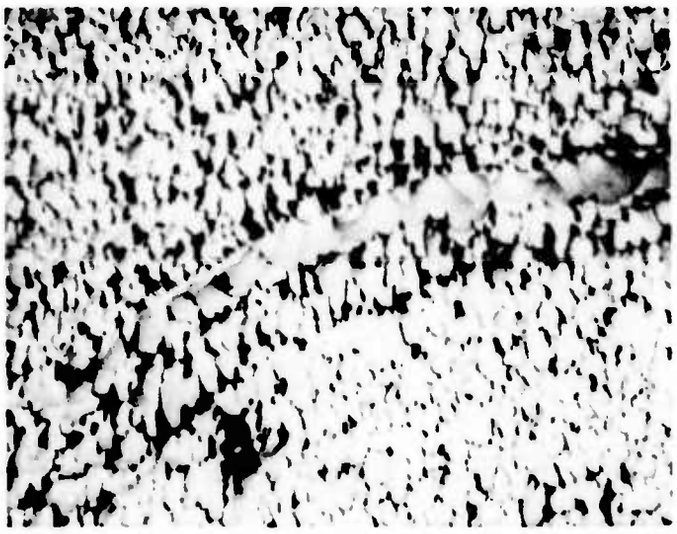
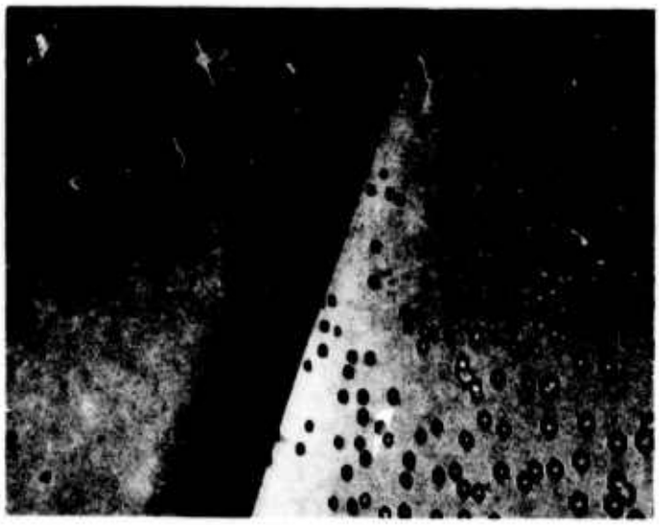


Figure 1. Surface of GaAs/GaAlAs
VR5-439/MRC 6074-1 50X

Figure 2. Surface of GaAs/GaAlAs
VR5-438/MRC 6074-1, 200X

(a)



(b)

Figure 3. Surface of GaAs/GaAlAs, VR5-440/MRC 6074-1. (a) 50X showing large plates up to 48 μm high which nucleated immediately along apparent scratch lines and other imperfections as well as smaller plates which must have nucleated at a later stage. (b) 500X showing tiny, late nucleating poly-hedra on bare substrate beside edge of a large plate.

3.0 LIQUID PHASE EPITAXY

3.1 Introduction

The primary objective of the Liquid Phase Epitaxy (LPE) portion of the program has been to grow GaAlAs epitaxial layers on GaAs substrates. An epitaxial layer of GaAs was then grown on the GaAlAs surface by VPE to complete the waveguide structure.

A detailed technical description and performance data of the LPE GaAlAs system were given in the July Semi-Annual Technical Report.

3.2 Experimental Results

No new GaAlAs epitaxial growth runs were made during this reporting period because of the difficulty experienced with the VPE growth of GaAs on the GaAlAs already available, as described in Section 2.0. A series of samples with imperfect surfaces, however, were polished and etched to supply material for experimental VPE GaAs growth runs to establish the proper growth conditions.

3.3 Conclusions

The LPE portion of this program has been suspended indefinitely for three principal reasons: (1) The growth of large area GaAs/GaAlAs structures has been found significantly more difficult than the growth of GaAs/GaAsP structures. (2) The attenuation rates observed in GaAs/GaAsP structures have been found to be at least equivalent to the best results obtained in any laboratory using GaAs/GaAlAs. (3) By suspending the LPE portion of this program it will be possible to concentrate more attention on the technologically more advanced GaAsP system.

4.0 WAVEGUIDE EVALUATION

4.1 Attenuation Measurements on GaAs/GaAsP Waveguides

No definitive new results have been obtained from waveguide attenuation measurements. The new samples of GaAs/GaAsP waveguides which were submitted for evaluation were not suitable for detailed attenuation measurements. Light could not be excited in one sample. For the other samples, light was coupled in and out with very low efficiency, and two output beams were observed from the edges instead of the center of the output prism, no matter how we adjusted it. (The prism base is smaller than the sample size.) This is apparently caused by the fact that the films werewarped. The surface is concave if viewed from the top. This curvature explains the existance of two output beams, because the prism edges have closer contact with the concave surface and the coupling condition is satisfied there. By reducing the waveguide sample width (for example. 5mm wide, with a prism coupler 15mm wide), light was coupled in and out, and the output beam was coupled out from the center of the prism. Two peaks were still observed but they were much closer. Attempts were made to measure the attenuation rate. Our preliminary result establishes an upper limit on the loss of 4 db/cm. Reliable results on attenuation could not be obtained because of the coupling problems caused by the bonding of the specimens. Thus, it could not be established whether the attenuation is comparable to the values of 1-2 db/cm obtained for similar structures reported in Semi-Annual Technical Report No. 2. Nevertheless the results obtained do indicate that large area, high quality films will be obtainable when the surface bow effect is reduced or eliminated.

4.2 Electro-Optic Modulation

No new results in the electro-optic modulation experiments were obtained. We expect new results will be obtained as soon as good quality and large samples of GaAs/GaAsP waveguide become available. A contributed paper, based on our preliminary result reported in our last Semi-Annual Report and entitled "Electro-Optic Modulation at 10.6 μm in Epitaxial GaAs Waveguides," was presented in the Topical Meeting on Integrated Optics to be held in New Orleans January 21-24, 1974.

4.3 Experimental Fabrication of Two-Dimensional Waveguides

Low loss two-dimensional waveguides have been successfully chemically etched. Our measurements demonstrate that the attenuation rate for two dimensional waveguide can be as low as that for one-dimensional waveguides. It is important to realize that a smaller r.f. power is required to drive the two-dimensional electro-optic modulator.

For the sample VR5-422 the measured attenuation rate for the TE_0 mode is 4.1 db/cm while the attenuation rate for TE_1 mode is 5 db/cm. These measurements are for one dimensional guide before etching.

Subsequently, the sample is first spin coated with liquid SiO_2 0.15 μm thick, and then spin coated with AZ 1350 photoresist, about 0.5 μm thick. AZ 1350 is exposed in the usual manner through a suitable photo-mask (made by conventional photolithography technique) to make an SiO_2 mask that will protect the white areas in Figure 4 during chemical etching. Following that the GaAs (dark area in Figure 1) is etched about 25 μm deep by H_2SO_4:H_2O_2:H_2O (3:1:1) at 45°C for about five minutes; the SiO_2 mask is then removed by HF.

The resultant product schematically shown in Figure 4 consists of a two-dimensional waveguide surrounded by deep etched grooves to isolate the waveguide from the surrounding mesa of GaAs. The two-dimensional waveguide has tapered transitions at both ends so that one dimensional waveguide modes can be excited by the prism coupler and that the taper will make a smooth transition from the one dimensional waveguide modes to the two dimensional waveguide modes. The surrounding mesa of GaAs is necessary to support the pressure of the prism coupler. The vertical deep groove cutting across the mesa shown in Figure 4 is necessary to prevent radiation leaking from the input prism coupler to the output prism coupler through the surrounding mesa of GaAs. Figure 5 shows a 500X magnification of a section of the etched waveguide where each large scale division corresponds to 2.2 μm in distance. Figure 6 shows the profile of the waveguide monitored by Dektak. The surface irregularities caused by chemical etching is clearly much less than 1 μm.

We have been able to excite several E^y_{1q} and E^y_{2q} modes by setting the vertical angle of incident CO_2 beam with the input prism for m = 0 and m = 1 modes of one dimensional waveguide. Modes having various values of q, the transverse mode order along the width of the two dimensional waveguide, were excited by adjusting the horizontal angle between the input prism and the axis of two-dimensional guide. When attenuation rates of the two-dimensional guide were evaluated by sliding the output prism coupler, we obtained 3.8 db/cm for E^y_{1q} modes and 4.9 db/cm for E^y_{2q} modes for small values of q.

This result demonstrated that no measurable increase in attenuation occured for the two-dimensional waveguide modes E^y_{1q} and E^y_{2q} (with small k values) as compared to the TE_0 and TE_1 one-dimensional waveguide modes. The slight decrease in attenuation is probably caused by the fact that we have chosen a better section of the sample to make two-dimensional waveguide. Similar results were obtained in sample No. VR5-424 where a 50 μm wide two-dimensional waveguide is fabricated. However, when a 25 μm wide two-dimensional waveguide is fabricated on Sample No. VR5-421 an increase of attenuation of 1 db/cm occurred for the E^y_{1q} modes and an increase of attenuation of 6 db/cm occurred for the E^y_{2q} modes.

4.4 Theoretical Calculation of r.f. power dissipation of the Electro-Optic Modulator

The theoretical calculation studies the waveguide structure shown in Fig. 7a. From static field considerations, with layer lengths $\ll \frac{\lambda r.f.}{4}$ (i.e. << 22 cm at 100 MHz) each layer of the electro-optic moudlator may be regarded as a parallel combination of lumped circuit elements R and C, in which we have assumed the layer medium to be homogeneous and have neglected the layer edge effect. The r.f. equivalent circuit of the modulator is shown in Fig. 7b The lumped circuit elements are given by:

$$C_i = \frac{\epsilon_i A}{d_i}$$

$$R_i = \frac{d_i}{A\sigma_i}$$

where ϵ_i is the permittivity, A is the cross sectional area, d_i is the layer thickness and σ_i is the conductivity which is related to the carrier concentration N by $\sigma_i = qN_i\mu_e$ with q the electron charge and μ_e the electron mobility. Only the GaAs waveguide layer has an appreciable resistance and virtually all the electric field appears uniformly across this layer. This resistance, R_2, should be as large as possible to minimize the power dissipated as heat within the device. With Rs as the source resistance, the bandwidth of the modulator is given by:

$$\Delta W = \frac{1}{(R_s \| R_2)C_2} R_s$$

would be small to increase the bandwidth within the constraints imposed by the required modulating field and the maximum power available from the source. For a 10 watt source with 50 Ω impedance, we have calculated the available electric field and the r.f. power dissipation in the GaAs layer. The results are shown in Table XI, with the carrier concentration as a variable. It is clear that a high resistivity GaAs layer is essential for the electro-optic moudlator.

A similar lumped element equivalent circuit for a Schottky barrier modulator is shown in Figure 8. For a reverse bias voltage, the modulating layer becomes depleted resulting in an effective capacitance with no parallel resistance. It allows us to create the electro-optic effect without excessive modulation power dissipation in the waveguide. Since the source for the modulator drives a capacitive reactance, the bandwidth is given by:

$$\Delta\omega = \frac{1}{R_s C}$$

where C is the effective capacitance of the depleted layer and R_s is the source resistance. Power required for $\Delta\omega$ while maintaining full depletion is shown in Figure 9.

4.5 Conclusions

1. No new results in waveguide attenuation measurements were obtained because of the surface bow effect.

2. Experimental fabrications of two-dimensional waveguides were successful. The attenuation rate for a two-dimensional waveguide as low as that for a one-dimensional waveguide is achievable.

3. Theoretical calculation of the r.f. power dissipation of the electro-optic modulator has been initiated.

TABLE XI

The Power Dissipation in GaAs Layer Driven
by a 10 Watt Source with 50 Ω Impedance

n/cc	Vapl Volts	E_{max} V/cm	ΔW	P_d Watts
10^{14}	0.27	385	10^{10}	4.99
10^{13}	0.85	1.2×10^3	10^9	4.94
10^{12}	2.7	3.8×10^3	10^8	4.92
10^{11}	7.9	1.1×10^4	1.8×10^7	4.36
10^{10}	17.2	2.4×10^4	3.8×10^6	4.06
10^9	21.6	3.1×10^4	2.4×10^6	0.64
10^8	22.3	3.2×10^4	2.2×10^6	0.03

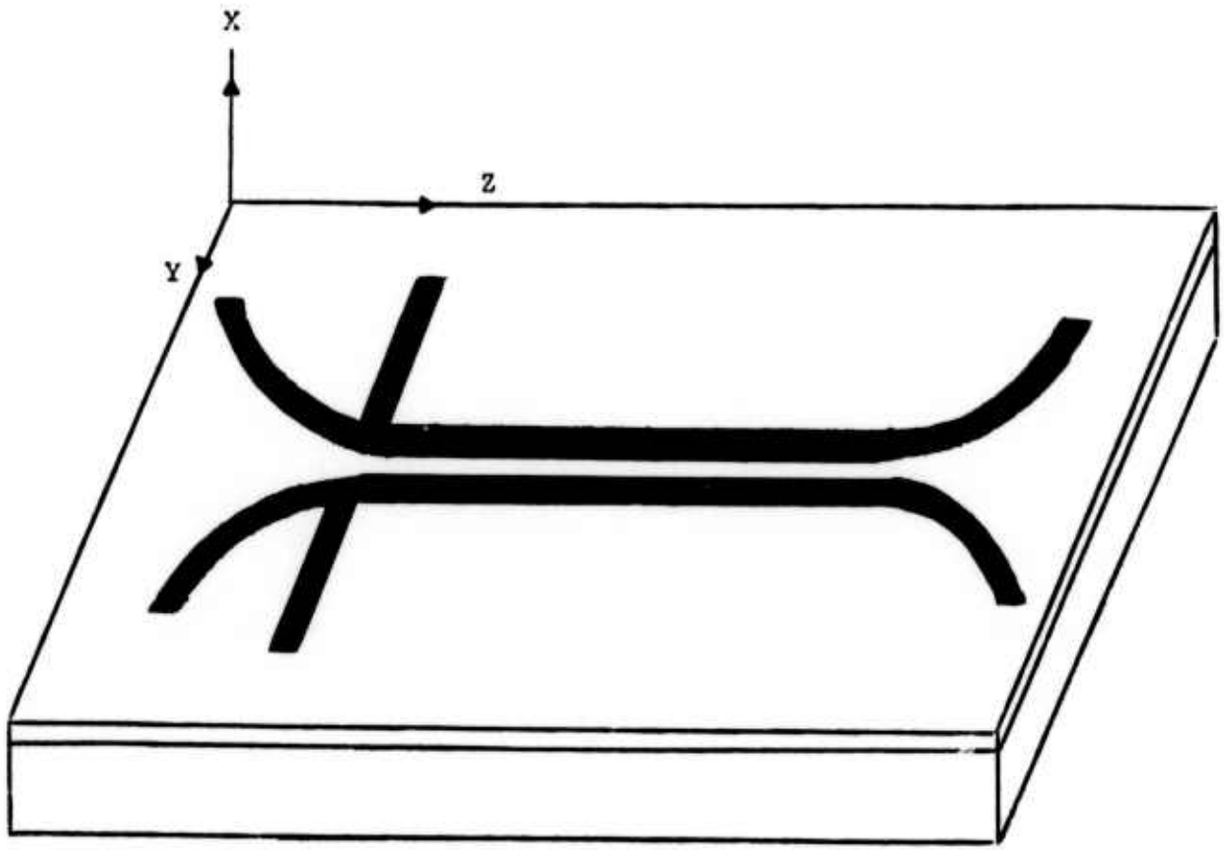


Figure 4. Schematic Diagram of an Etched Two Dimensional Waveguide.

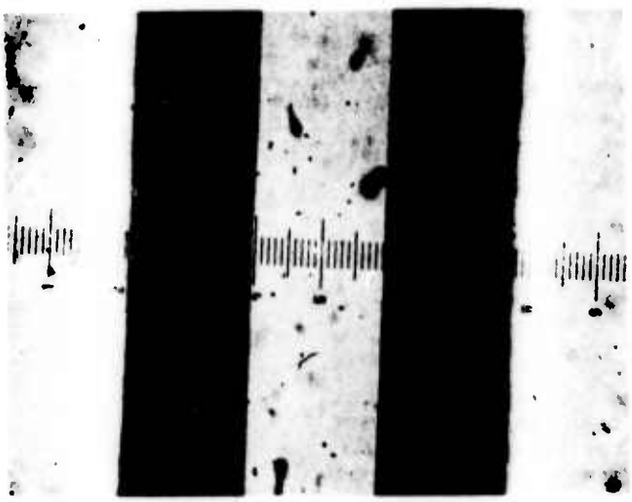


Figure 5. Photograph (500x) of a Part of the 50μ Wide Two Dimensional Waveguide Fabricated on VR5-422.

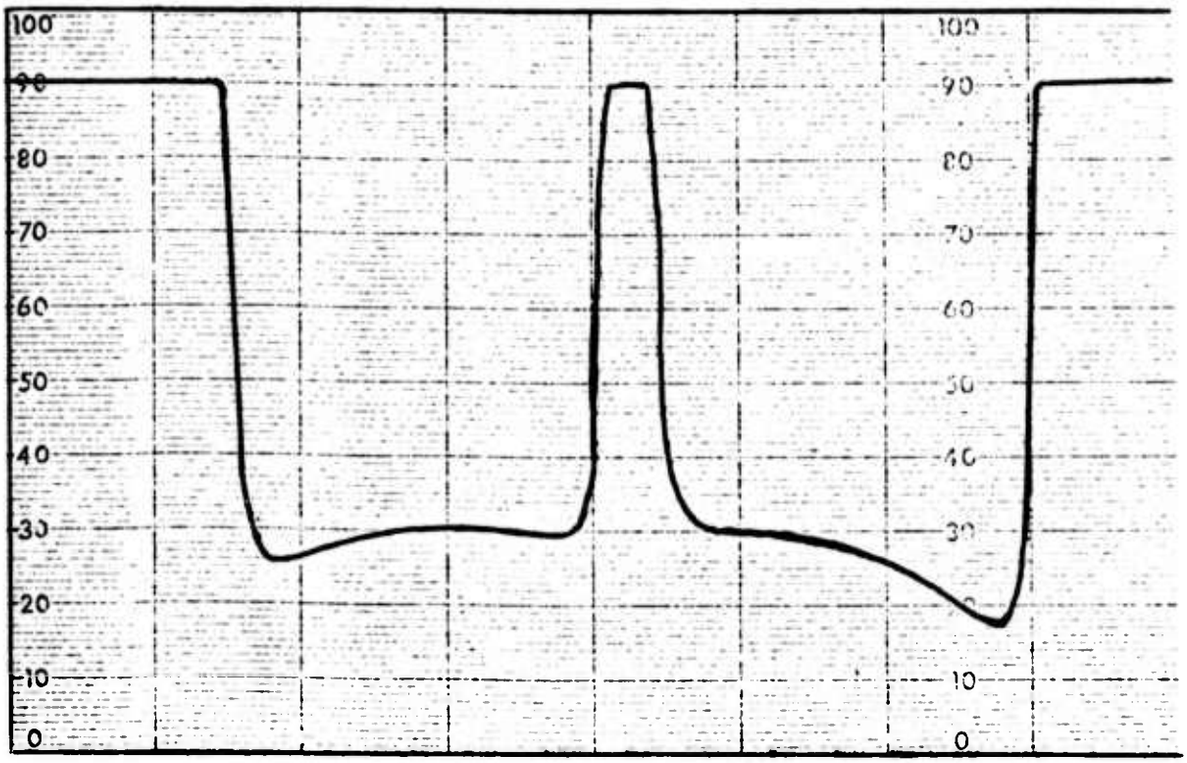
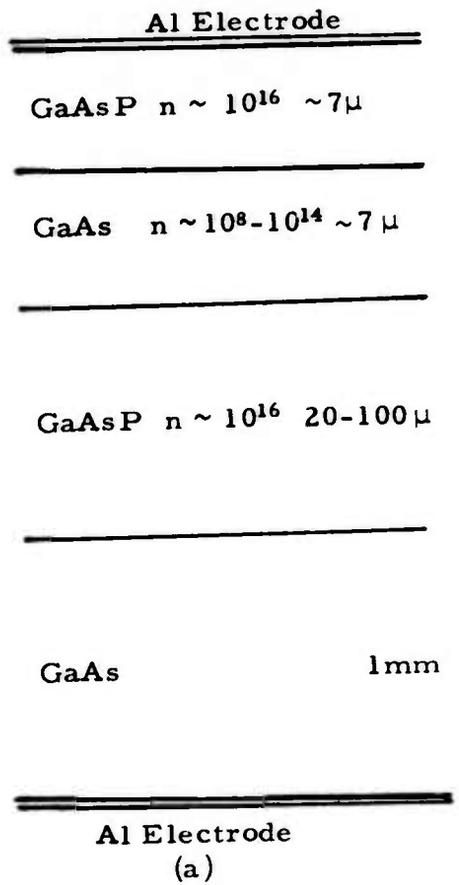
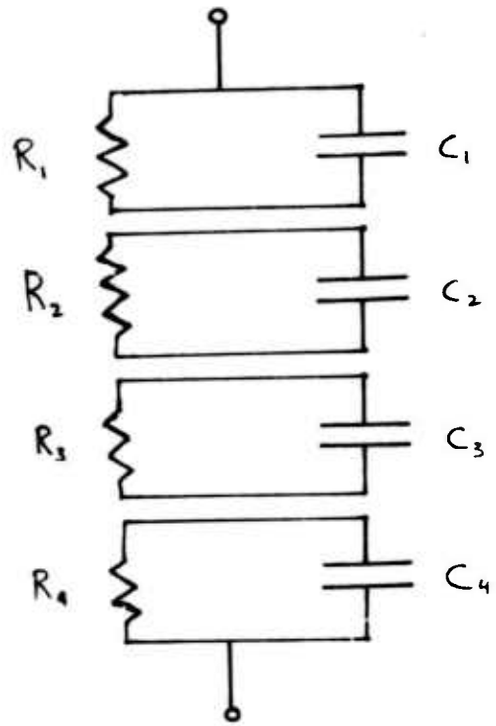


Figure 6. Dektak Trace Showing Profile of the 50μ Wide Two Dimensional Waveguide. Horizontal Magnification 100, Vertical Full Scale 50μ.



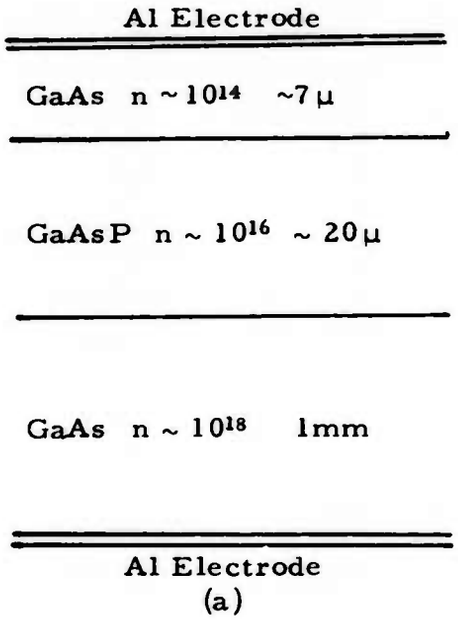
(a)



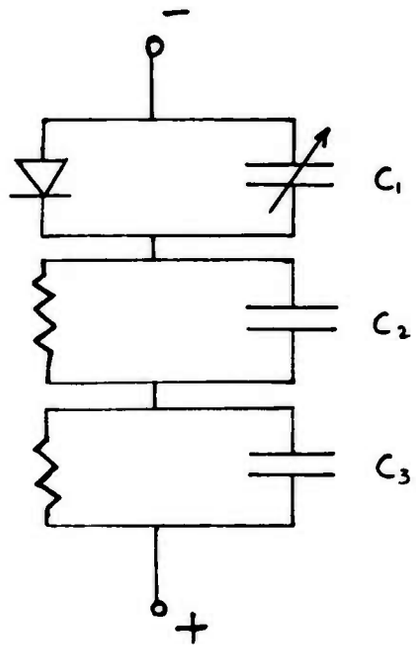
(b)

Figure 7. (a) Waveguide Electro-optic Modulator Geometry

(b) Its r.f. Equivalent Circuit



(a)



(b)

Figure 8. (a) Schottky Barrier Modulator Geometry

(b) Its r.f. Equivalent Circuit

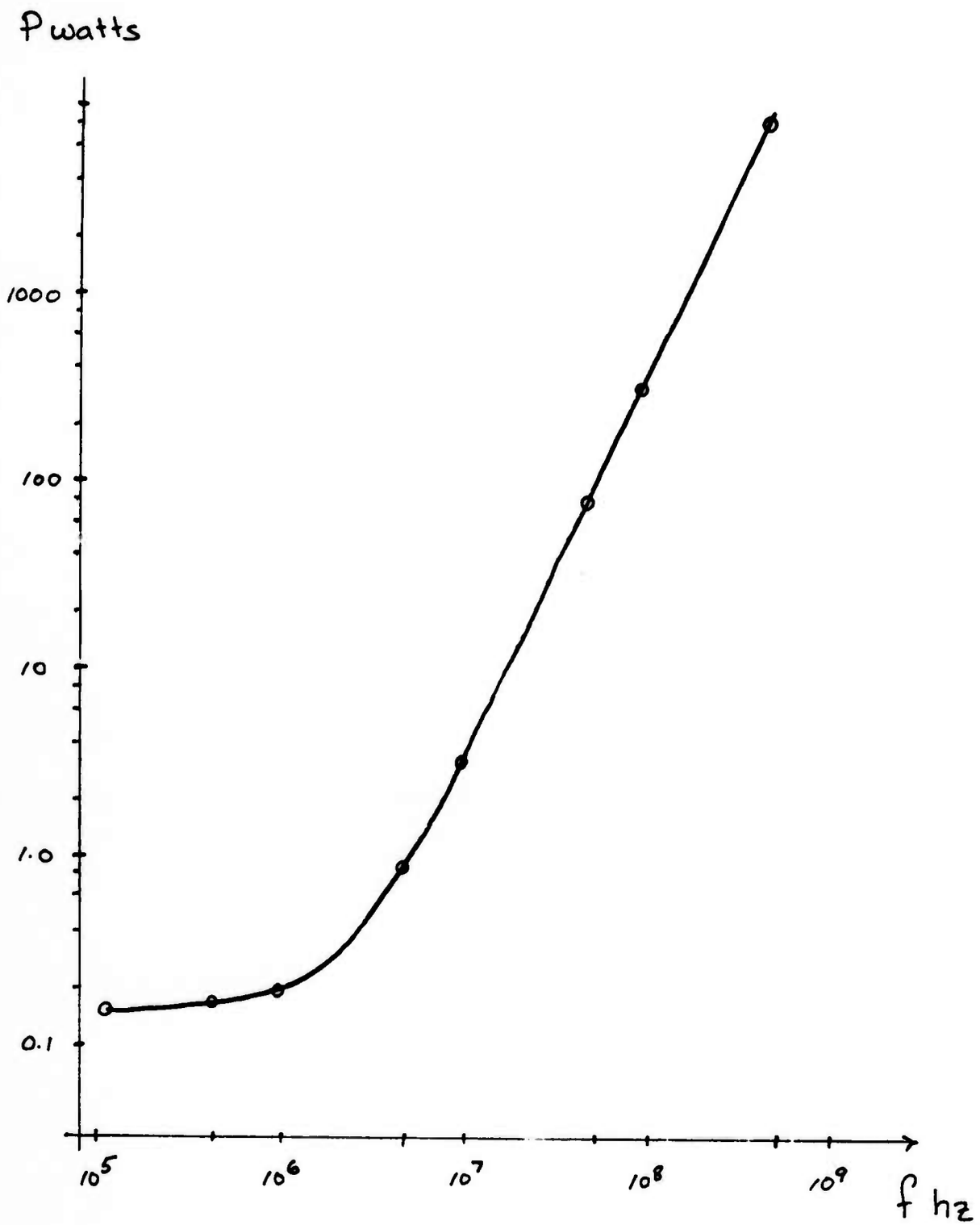


Figure 9. Device driven by a current source paralleled with 50 Ω
Power dissipated through 50 Ω to maintain full depletion (3.9V)